BME Capacitor Risk Management

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This work was performed at the Jet Propulsion Laboratory, California Institute of Technology,
Under contract with the National Aeronautics and Space Administration (NASA)

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Managing risk always involves managing the entire reliability lifetime of a device:

- **Early life:** Screening
- **Useful life:** Low levels of defects
- **End of life:** Physics of Failure
BMEs and FPGAs

Our goal is to manage the risk of using Xilinx Virtex 4 and 5 FPGAs made with BME capacitors
AVX BME Caps used on Xilinx FPGAs - Optical
AVX BME Caps used on Xilinx FPGAs - SEM
Multilayer ceramic capacitor (MLCC)
- Alternating layers of dielectric and electrode
- Used throughout electronics industry

Historically these type of capacitors used PME = Precious Metal Electrodes (usually palladium).

Pd prices jumped from $100/ounce to $1500/ounce in 1990’s.
- Also demand for cheap electronics drove capacitor prices down.

BME = Base Metal Electrode (usually nickel) developed as cost and performance solution
What about the dielectric?

- MLCC dielectric of choice for both PME and BME is BaTiO$_3$
  - High melting point: 1625° C (good for stable manufacturing)
  - Ferroelectric: High dielectric constant ~3000 (helps volumetric efficiency)
  - Perovskite structure: allows for many dopants/stoichiometry to customize thermal, electrical, manufacturing and reliability performance

- **Changing electrodes but keeping the dielectric the same requires a change to the manufacturing processing.**

- **PME** were sintered/fired in air atmosphere
  - Pd Electrodes will not oxidize
  - Produces favorable electrical properties

- **BME** must be sintered in reducing (i.e. vacuum, forming gas) atmosphere
  - Ni Electrodes will oxidize in air
  - Interface capacitance will dominate performance
  - Dielectric turns to semiconductor

- **No free oxygen/reduction atmosphere => oxygen vacancies in dielectric film**
  - Degrades internal resistance and long term reliability

- **Additional dopants must be added and new re-oxidation process added to BME to address oxygen vacancies.**
Examples of Oxygen Vacancies in BaTiO$_3$

- Intermediate ionic radius rare-earth (Dy, Ho, Er) show smaller aging rates than large radius (La, Sm, Gd)
- DC bias drives oxygen vacancies to cathode/ceramic interface
  - Degrades insulation resistance
BME Performance Concerns

Variation among vendors (same 16V/1uF capacitor)

Logarithmic degradation over time.

\[ \frac{C(t)}{C(0)} = 1 - k \log(t) \]

15 year missions could have 20 decades of operation => final value is ~35% of t=0 value

Novak DesignCon 2011
• **Insulation Resistance = applied voltage/leakage current**

• **As time increases, electromigration of oxygen vacancies from core to interface across grain boundaries**
  – Decreases resistivity
  – Tunneling current through grain boundaries

• **Pile up of oxygen vacancies finally decreases resistivity to critical level**
## Manage Risk with Likelihood and Consequence Matrix

### Table:

<table>
<thead>
<tr>
<th>Likelihood</th>
<th>Consequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>&gt;50%</td>
</tr>
<tr>
<td>4</td>
<td>&gt;10%</td>
</tr>
<tr>
<td>3</td>
<td>&gt;1%</td>
</tr>
<tr>
<td>2</td>
<td>&gt;0.1%</td>
</tr>
<tr>
<td>1</td>
<td>&lt;0.1%</td>
</tr>
</tbody>
</table>

### Consequence:

- **Minimal degradation, circuit performance not affected**
- **Parametric degradation, degraded circuit performance**
- **Part Failure, circuit failure. Mitigation scheme to restore**
- **Part failure/circuit failure. No mitigation scheme**
- **Part Failure/Circuit Failure. Failure of adjacent circuits**

### Likelihood:

- Minimal degradation, circuit performance not affected
- Parametric degradation, degraded circuit performance
- Part Failure, circuit failure. Mitigation scheme to restore
- Part failure/circuit failure. No mitigation scheme
- Part Failure/Circuit Failure. Failure of adjacent circuits

### Consequence:

- 1
- 2
- 3
- 4
- 5
Determine Capacitor & System Reliability Requirements

Capacitor System Reliability = Component Reliability^# of capacitors

<table>
<thead>
<tr>
<th># of caps</th>
<th>Capacitor Reliability</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.9900  0.9990  0.9999  1.0000</td>
</tr>
<tr>
<td>5</td>
<td>0.9510  0.9950  0.9995  1.0000</td>
</tr>
<tr>
<td>10</td>
<td>0.9044  0.9900  0.9990  0.9999</td>
</tr>
<tr>
<td>15</td>
<td>0.8601  0.9851  0.9985  0.9999</td>
</tr>
<tr>
<td>20</td>
<td>0.8179  0.9802  0.9980  0.9998</td>
</tr>
<tr>
<td>25</td>
<td>0.7778  0.9753  0.9975  0.9998</td>
</tr>
<tr>
<td>30</td>
<td>0.7397  0.9704  0.9970  0.9997</td>
</tr>
</tbody>
</table>

JPL needs capacitors with 4 to 5 9’s reliability at the END of mission life to have a low likelihood rating.
Sample Size Requirements

Percent Defective (ppm) vs Sample Size vs Confidence Limit

Current life test have sample size variation

<table>
<thead>
<tr>
<th>Xilinx Part #</th>
<th>Cap Size</th>
<th>Life Test Voltage (V)</th>
<th>Total</th>
<th>Fails (0 to 2000 hr)</th>
<th>Fails (2000 to 4000 hr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCC0013</td>
<td>0508</td>
<td>6</td>
<td>259</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>BCC0014</td>
<td>0508</td>
<td>9.45</td>
<td>138</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>BCC0019</td>
<td>0306</td>
<td>6</td>
<td>91</td>
<td>2*</td>
<td>0</td>
</tr>
</tbody>
</table>
### COTS FIT Rates

**Mission Assurance Office**

**Section 514**

**USA / El Salvador / Malaysia**

**RELIABILITY ENGINEERING**

**QUARTERLY RELIABILITY SUMMARY**

1st QUARTER 2011

**PRODUCT:** MULTILAYER CERAMIC CAPACITORS

**TEST CONDITIONS:** 2X-RATED VOLTAGE DC MINIMUM
MAXIMUM RATED TEMPERATURE

<table>
<thead>
<tr>
<th>DIELECTRIC GROUP</th>
<th>LOTS TESTED</th>
<th>PIECES TESTED</th>
<th>DEVICE HOURS</th>
<th>EQUIVALENT DEVICE HRS</th>
<th>FAILURE RATE (1/1)</th>
<th>EQUIVALENT DEVICE HRS</th>
<th>FAILURE RATE (1/1)</th>
<th>FAILURE RATE FITS - (2/1)</th>
<th>MTBF</th>
</tr>
</thead>
<tbody>
<tr>
<td>NPO/COG</td>
<td>230</td>
<td>29170</td>
<td>2.87 x 10^6</td>
<td>2.30 x 10^7</td>
<td>0.010</td>
<td>1.84 x 10^11</td>
<td>1.25 x 10^-6</td>
<td>0.013</td>
<td>7.99 x 10^10</td>
</tr>
<tr>
<td>X7R</td>
<td>659</td>
<td>104191</td>
<td>1.21 x 10^7</td>
<td>9.64 x 10^7</td>
<td>0.013</td>
<td>7.71 x 10^11</td>
<td>1.68 x 10^-6</td>
<td>0.017</td>
<td>5.94 x 10^10</td>
</tr>
<tr>
<td>X5R</td>
<td>26</td>
<td>3008</td>
<td>2.89 x 10^5</td>
<td>2.31 x 10^6</td>
<td>0.100</td>
<td>1.04 x 10^9</td>
<td>2.22 x 10^-4</td>
<td>2.216</td>
<td>4.51 x 10^8</td>
</tr>
</tbody>
</table>

**NOTES:**

1/ Failure Rates are calculated in Percent Per 1000 Hours at 90% Confidence Level
2/ 1 FIT = 1 Failure in 10^9 Hours (PPM per 1000 Hours) at 90% Confidence Level

<table>
<thead>
<tr>
<th>Hours</th>
<th>0.1</th>
<th>1</th>
<th>10</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>1.0000</td>
<td>1.0000</td>
<td>1.0000</td>
<td>0.99999</td>
</tr>
<tr>
<td>1000</td>
<td>1.0000</td>
<td>1.0000</td>
<td>0.99999</td>
<td>0.99990</td>
</tr>
<tr>
<td>8760</td>
<td>1.0000</td>
<td>0.99999</td>
<td>0.99991</td>
<td>0.99912</td>
</tr>
<tr>
<td>43800</td>
<td>1.0000</td>
<td>0.99996</td>
<td>0.99956</td>
<td>0.99563</td>
</tr>
<tr>
<td>87600</td>
<td>0.99999</td>
<td>0.99991</td>
<td>0.99912</td>
<td>0.99128</td>
</tr>
<tr>
<td>131400</td>
<td>0.99999</td>
<td>0.99987</td>
<td>0.99869</td>
<td>0.98695</td>
</tr>
</tbody>
</table>

- **COTS AVX data shows strong dependence on dielectric.**
- **Space dielectric does not have this large database to leverage.**
Life Test Requirements

\[ \frac{t}{t_0} = \left[ \frac{V}{V_0} \right]^n e^{\left( \frac{E_a}{k} \left( \frac{1}{T} - \frac{1}{T_0} \right) \right)} \]

- \( T_0 \) and \( V_0 \) are life test conditions
- \( T \) and \( V \) are mission conditions
- \( t = \text{mission life}, t_0 = \text{life test duration} \)
- \( E_a = 1.03 \) and \( n = 4.6 \)

**Hours of 125C Life Test Required to Ensure 10 yrs of life at 3.4V for Various Temperatures & Voltage**

- **4V**
- **6V**
- **Xilinx Life Test**
IR Degradation Life Test Analysis

1.00E+06 1.00E+07 1.00E+08 1.00E+09 1.00E+10

Insulation resistance (Ohms)

Hours of Operations (Arbitrary)

Life Test I - 20 to 50% degradation region (unknown effect on AC device performance)

Life Test II – 100X to 1000X degradation region. FPGA is expected to fail due to high current conditions
Life Test Predictions for Operational Conditions
FPGA Power Distribution Network

- High speed (>100MHz) operation requires sophisticated signal integrity management
- Maintain low impedance path from FPGA to supply through die, package, and PCB.
  - Different regions have frequency response ranges
  - Compensate for large swings in current until Vsupply can respond
- BME caps on FPGA
  - Power/GND plane decoupling
  - Filtering
  - Series DC blocking for Gbit/sec links
- **What happens to PDN when BME degrades?**
Effect of ESL Change on 0306

Mission Assurance Office
Section 514

C = 1.0 μF, ESR = 0.004 ohm, L = 1, 35, 100 pH

\[ Z_C = R + j \left( \omega L - \frac{1}{\omega C} \right) = \text{Re}\{Z_C\} + j \text{Im}\{Z_C\} = R + jX \]

Istavan novak
Summary

• Integrate reliability function of BME into FPGA reliability function with risk matrix.
• Significant sample size required to resolve acceptable levels of defects.
• Long term (> 1khrs) needed to cover long term high temperature mission operation.
• HAST/HALT data needed on exact space BME caps for operational predictions.
• Electric field based specifications are required to advance BMEs for general purpose use.
• Impact of the electrical degradation of the BME cap on FPGA performance is required portion of overall risk plan.