Comparing Ground and On-Orbit Test Results for Xilinx SRAM FPGAs

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LANL’s 40+ Years in Space

- LANL has been involved in space systems and science since 1963 with the Vela program
  - 1400 sensors, 400 instruments, 60 satellites

- DOE-Sponsored Space Nuclear Detonation Detection Program and Related Technologies
  - Advanced Space Computing Work: 25 people involved, multi-year effort
  - Partners: Sandia National Laboratories

- LANL has an end-to-end capability.
  - Systems Engineering and Mission Design
  - End-to-end Satellite Design, Fab, Testing, Deployment, Ops
  - Satellite Command & Control
  - Ground Station Development & Operation
  - Knowledge Extraction/In-Situ Computation
  - System & Data Management
  - Flight FPGA Experimentation & Development
  - Software Engineering
Science and national security concerns move at a rapid pace. Space assets must be flexible enough:
- To take advantage of the latest science to improve performance for existing science and national security missions and
- To address new missions for the ever changing needs of science and national security.

The amount of data collected by sensors grows at a faster rate than the bandwidths of downlinks.
- On-orbit processing needed to reduce data downlink requirements
- Otherwise, all collected data not exploited, missing important discoveries or events.

High-performance on-orbit computing can enable new approaches and lead to new science
- Intelligent sensor cueing, array signal processing, multi-sensor data fusion, high-resolution detection, classification, and collection
LANL’s Solution to World-Class On-Orbit Computing Using COTS

- Use commercial-based technologies for high performance portions of the space systems
  - Use fault-tolerant design at the system, module, and micro-architectural levels with SRAM-based field-programmable gate arrays (FPGAs) to provide the robustness needed for the system without “over-engineering” systems
  - Use more conventional radiation-hardened technologies in high-risk portions of the system or where performance and cost are not drivers

- LANL FPGA methodology:
  - Characterize both the FPGAs and the user circuits
  - Mitigate user circuits to SEUs through a combination of partial triple-modular redundancy, logical constant removal and scrubbing
  - Leverage fault injection and modeling tools for on-bench testing in the design phase
  - Leverage radiation testing and in-payload fault injection for hardness assurance testing of the final design

LANL-Developed FPGA CAD Tool Flow for Highly Reliable FPGA Designs for Space (Green, Light Blue tools developed under SOPraNo/DAPS/CFE)
First On-Orbit Demo Flying Since March 2007: Cibola Flight Experiment

- **Software Defined Radio**
  - Four channels, 20 MHz bandwidth each tunable from 100 to 500 MHz,
  - 3-board, 9 Xilinx Virtex FPGA 300-Gop/sec(peak) re-configurable computer (RCC)
  - Real-time detection, geo-location, compression of wide-band RF signals

- **Orbit is 560 km with a 35° inclination**

- **Validated approach for using high-performance COTS FPGAs and other devices in space**
  - >10,000 experiments
  - 1000s of hours of operation
  - Fault tolerance found effective
  - New app development still active
At launch we were in solar min & expected ~1 SEU/day

We have since transitioned to solar max & expectations decreased to ~0.75 SEU/day

We prepared for the worst.
CIFE Performance

- Actual SEU rates have been much lower:
  - During solar min, there was on average 0.25 SEUs/device-day and often went days without SEUs
  - Since transitioning to solar max, SEU rates have decreased by 1/3 and often now go a week or more without SEUs
  - We are currently making a deep dive through the data to see if operational decisions have caused the SEU rate to be unnaturally lower than expected

- In general, CFE’s low altitude and inclination provided a benign environment for the Virtex FPGAs, as the spacecraft transits only a small portion of the South Atlantic Anomaly
Second On-Orbit Demo Flying Since 2011: Mission Response Module

- Software Defined Radio from CFE was updated and miniaturized:
  - 9 Virtex → 2 Virtex
  - There are two units, called LEUs:
    - LEU1: technology readiness application
    - LEU2: SDR application

- Orbit is more aggressive, although operational issues are definitely lowering SEU rates in the system
**MRM Predictions**

- Information from Greg Allen's “Virtex-4QV Static SEU Characterization Summary” was used to calculate the CREME96 predictions
  - For this orbit, CREME96 predicted a combined FPGA SEU rate of 68-89 SEUs/device-day for each LEU, depending on solar conditions.
  - Each Virtex-4 should have an observable output error approximately every 15 to 25 days.

- There was some concern before launch that MBUs could limit the effectiveness of TMR.
  - LANL test results indicated that $3.25\% \pm 0.05\%$ of all SEUs caused by 63.3 MeV protons would be MBUs.
  - Configuration memory could have up to $6.75\% \pm 0.10\%$ MBUs.
  - In heavy ions, the MBU rates could be much higher.

- The actual SEU rate has been between 20-25% of the predicted SEU rate
  - The LX FPGA has $14.5 \text{ SEUs/device-day} \pm 0.07 \text{ SEUs/device-day}$.
  - The SX FPGA has $5.2 \text{ SEUs/device-day} \pm 0.08 \text{ SEUs/device-day}$.

- Due to operational issues, we are missing some of the transit in the SAA
  - When this is taken account of, the predictions are closer to 50%
  - We believe the other 50% could be caused by several centimeters of Al against the interior-facing side

- There have been four output errors since October 2011 – an immunity to over 99% of all SEUs
Locations of SEUs

Most SEUs occur in the SAA. We often get up to 5 SEUs for each pass through SAA.

Most MBUs occur in the SAA.
Multiple-bit Upsets

- We determined that $7.22\% \pm 0.76\%$ of the on-orbit SEU events are MBUs.
  - None of the output errors have been tied to MBUs.

- The data from all of the FPGAs is consistent with normal incidence 63.3 MeV proton tests.

- CREME96 predicts the MBU rate as 1.18 MBUs/device-day for the SX FPGA and 3.31 MBUs/device-day for the LX FPGA.
  - When derated for operational usage, the MBU rate for the SX FPGAs is 6.5% and 6.6% for the LX FPGAs.

- On average $85\% \pm 15\%$ of the MBUs are 2-bit upsets.

<table>
<thead>
<tr>
<th>Component</th>
<th>MBUs</th>
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<tbody>
<tr>
<td>LEU1 LX</td>
<td>7.59% ± 1.13%</td>
</tr>
<tr>
<td>LEU1 SX</td>
<td>7.35% ± 1.32%</td>
</tr>
<tr>
<td>LEU2 LX</td>
<td>6.51% ± 2.06%</td>
</tr>
<tr>
<td>LEU2 SX</td>
<td>5.19% ± 2.41%</td>
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What’s Next?

- We’re actively moving forward in three different directions:
  - Continued experimentation with Virtex-7
  - Upcoming operational missions with both the radiation-hardened by design (RHBD) Virtex-5 and Spartan-6

- We’re tailoring systems to mission needs and requirements:
  - Low-criticality missions with short duration missions will use Spartan-6 and the Actel ProASIC 3
  - High-criticality missions with long duration missions will use RHBD Virtex-5 and Actel RTAX
  - In between the two extremes, we may use Virtex-7 with Actel ProASIC3

- There might also be the possibility of using the newer Altera Stratix parts – Stratix-IV is the first modern Altera part that does not latchup and Stratix-V supports partial reconfiguration which can be used for scrubbing
Conclusions

- LANL has had two successful space experiments using the Virtex and Virtex-4:
  - Both systems had SEU rates that were lower than predicted.
  - Both systems have very few operational issues due to the FPGAs.
  - The MBU rate for the Virtex-4 system is higher than the Virtex system, but has not caused an operational failures to date.

- In the future, LANL will continue to experiment with newer Virtex devices, as well as using the previous generation Spartan and Virtex FPGAs in operational missions.