Advanced Technology Group
Radiation Hardened Microelectronics Program:
A Status Report
Presented at the Annual
Microelectronics Reliability and Qualification Workshop

11-12 December 2012
RHM Branch Mission, Objectives & Applications

**Mission:** Develop both evolutionary and revolutionary microelectronics technologies to enhance satellite electronic systems capabilities

**Objectives:**
- **Onboard Processing (OBP) Enhancements:**
  - Provide heterogeneous OBP capability to support TFLOP performance & TB storage at reduced SWaP
  - Provide high performance analog/mixed-signal technologies to support communications and intelligence applications
- **Electronically Steerable Array (ESA) Enablement:**
  - Very high SFDR low power CNT FET technology for LNA, mixer and ADC designs
  - UDSM technology for elemental digital beam-forming

**Applications:**
- System survivability
- Pre-planned program upgrades by providing improvements in performance, reliability & SWaP
- New mission capabilities
Near Term Technology Program

Objective:
- Productization & Qualification of RH Electronics Technologies (250nm to 150nm)
- 10X improvement in OB processing performance

Tasks:
- RH15F Process Class V Qualification
- L2 Cache MCM/Synchronous SRAM Qualification
- 4Mb CRAM Qualification
- RH18/RAD750 200MHz/400MIPS Processor Qualification
- 100 MHz Bridge ASSP Development
- RAD750/250MHz 500 MIPS processor
- RH SERDES Development
- Structured Array Development
- Optimized SERDES Development
- Advanced Packaging Development
- HX-5000 SEE Characterization
Near Term Program Status
Balanced design to support > 400 MIPS Throughput

- L2 CACHE Memory Class Q Qualification Completed
- RAD750 200MHz/400MIPS Class Q Qual 4QCY12
- 100MHz Bridge Chip Class Q Qual 4QCY12
- RH 16Mb (X32) SRAM Class Q Qual 4QCY12
- RH SERDES Pass 2 Completed Class Q Qual 4QCY12
- RH 4Mb NVRAM Class Q & V Qual Completed
- RH15 Class V Qual Complete
- Structured Array Complete FPGA Replacement
- 5Gbps SERDES Design Complete Demo 2QCY13

Spacecraft Front-end & Processing

On Board Processing System

- General Purpose Processing
- Digital Signal Processing
- Command & Data Interface
- SpaceWire Router
- Data Storage Unit
Mid/Far Term Technology Program

**Objective:**
- Demonstration of technology to provide a heterogeneous, flexible > TFLOP OBP architecture to support full range of processing needs (MIPS to TIPS)
  - Adaptation of Commercial Processes & IP for Space Applications
  - >1000X in OB processing performance; > TFLOP OBP performance
- Demonstration of high performance AMS technology
  - GSPS wide-band ADC/DAC

**Tasks:**
- RHBD 90nm & 45nm 70/250GFLOP DSP
- RHBD Vector Processor Host Bridge
- RHBD 45nm Next Generation multi-core GPP Family
- RHBD 45nm ASIC Design, Demonstration and Qualification
- RHBD 45nm/32nm Next Generation Analog/Mixed-Signal Technology Development
- RHBD 90nm Reliability Investigation & QML Qualification Support
- RHBD Next Generation FPGA Investigation
The combination of a SOC proven 45nm ASIC library and improvements for radiation and reliability provide an extensive capability for demanding space missions.
**Mid/Far Term Program Status**

**RHBD < 90nm technology to support ESA, Signal Conversion, Data Storage & OBP Applications**

**RH OBP Board**
- 4-70/250 GFLOP DSPs + Host Bridge
- ~1TLOP Performance/BD
  (> TFLOP/Box)

**Spacecraft Front-end & Processing**

**RHBD 90/45nm GFLOP DSP**
- 70/250 GFLOP
- RHBD 90nm devices in test

**RHBD 90/45nm Mixed-Signal technology for SIGINT, ESA & COMM Applications**

**RHBD 45nm Mixed-Signal technology for SIGINT, ESA & COMM Applications**

**RHBD 45nm GPP**
- RAD55XX Family

**RHBD 45nm DSP Host Demo 4QFY14**

**Next Gen RH Reprogrammable FPGA**
- FY12 Architecture Investigation

**RHBD 45nm ASIC Design & Demonstration and Qualification Effort 4QFY14**
RHBD 90nm/45nm Onboard Processing & Control Technology Development & Demonstration Program

- **Program Objectives**
  - Design, development, demonstration and verification of a RH, flexible and heterogeneous architecture onboard processing capability to meet the full range of satellite payload processing and control function needs (MIPS to TIPS)

- **Technical Approach**
  - Combines advanced commercial DSP & GPP IP with RHBD 45nm technology to achieve program objectives
  - Develop and demonstrate:
    - GFLOP DSP (90nm mid term & 45nm far term)
    - Host Bridge to support TFLOP SBC capability
    - MIPS to GIPS GPP family
    - GPP SBC
    - RH DDRX Controller
The RA\textit{DS}P\textit{EED} DSP is a radiation hardened variant of the CSX700 digital signal processor (DSP) from ClearSpeed Technology.

- RA\textit{DS}P\textit{EED} DSP features @ 90nm
  - 160 (152 + 8 spare) processing elements (PE) in two multi-threaded array processors (MTAP)
  - Throughput: 70 GFLOPS @ 15 W power dissipation
  - Each PE incorporates double precision floating point hardware as well as integer processing
  - Single instruction, multiple data (SIMD) architecture
  - Dual ClearConnect™ bridges (CCBR)
    - Each with ~ 30 Gb/s throughput
    - Supports direct connection between DSPs or to a backplane using a bridge
  - Dual DDR2 DRAM interfaces
    - A DDR2 interface is dedicated to each MTAP, avoiding bottlenecks
    - Throughput: ~30 Gb/s each
- Supported by mature commercial software development kit
- Software prototyping hardware available now

The RA\textit{DS}P\textit{EED} DSP chip includes two independent cores, each with 76 parallel processing engines, and dual high performance memory and I/O ports.
Dual CCBR interfaces to RADSPREAD DSP chips (30 Gb/s each)
  - Full duplex double data rate wide parallel point to point connection
  - Four “x4” serial 3.125/5 GHz RapidIO 2.1 interfaces plus a spare x4 (40-64 Gb/s total)
  - Control Plane provided through SpaceWire interface
  - DDR2/3 SDRAM memory controller with SECDED ECC (up to 50 Gb/s)
  - Startup ROM and Flash controllers for interfacing with boot and non-volatile memory
  - Multiple 64-bit RAD5500™ Power Architecture processor cores:
    - Setup RADSPREAD DSP operations
    - Control data transfers to/from Serial RapidIO backplane
    - Supplement data processing where more efficient
  - Host debug port to RADSPREAD DSP and JTAG interface for debug and test
  - Real time trace provides access to internal nodes

The RADSPREAD-HB™ ASIC sets up the RADSPREAD DSP, provides a high speed path to and from a RapidIO backplane, and provides high performance general purpose processing.

RADSPREAD-HB status:
In design now
Prototypes: 2014

The RADSPREAD-HB is built upon Freescale QorIQ™ architecture
Processor Family Development – RAD 5545 – 32/64bit multi-core Processor

Based on the mature Freescale QorIQ™ architecture, the RAD5545 provides a 10X performance increase over the RAD750 while maintaining the heritage of the PowerPC software architecture and commercially available software development tools.

Features include:
- Up to four RAD5500™ cores
- Up to 5.6 Dhrystone GIPS
- Fully compatible with 32-bit software
- Dual DDR 2/3 DRAM interface
- Up to four “x4” RapidIO ports provide up to 64 Gbps I/O throughput
- Real time trace / debug
- SRAM / C-RAM interfaces
- Four port SpaceWire router
Based on the mature Freescale QorIQ architecture, the RAD5510 provides a 3X performance increase over the RAD750 and integrates the heritage bridge functions, while maintaining the heritage of the PowerPC software architecture and commercially available software development tools.

Features include:
- One RAD5500™ core
- Up to 1.5 Dhrystone GIPS
- Fully compatible with 32-bit software
- DDR2/3 DRAM interface
- SRAM / C-RAM interface
- Four port SpaceWire router
- PCI parallel bus
- NAND Flash controller
DSP Flight Board Block diagram & Model

Key components:
- RA\textsc{DSPEED} DSP
- RA\textsc{DSPEED}-HB
- DDR2 SDRAM
- Switching POL Regulators

Packing over 5 GIPS and 144 GFLOPS of Signal Processing accessed by four 16 Gbps Pipes, the RADSPEED DSP Flight will significantly increase onboard processing.
The Rad Hard By Design 45nm Library Development program provides the technology required for low power, high performance, high density ASIC solutions.
RHBD 45nm ASIC Development, Demonstration & Qualification Program

Program Objectives
- Development, demonstration, and Class Q/V qualification of a RHBD 45nm ASIC technology.

Program Tasks
- Radiation & Reliability Technology Assessment & Characterization
  - Reliability assessment and remediation
  - RHBD library development & demonstration
  - Radiation effects modeling and simulation
- RHBD ASIC Design and Demonstration
  - Design, fabrication and test of two ASICs
  - Package development and demonstration
- ASIC & Technology Qualification
  - QML Class V qualification
  - QML Class Q ASIC qualification
  - Design flow qualification
RH45 ASIC Library Description

Reliability Enhancements to RH45 ASIC library and custom circuitry
- Selective metal width updates and modifications for electro-migration (EM)
- Lower VDD (0.95V nominal) to limit NBTI/GOI effects
- Enhanced design methodology (e.g. power aware placement) for reduction of hot spots
- Power grid segmenting to control power and thermal profile
- Avoiding (and identifying / updating) circuit topologies that may impact reliability (e.g. voltage stacks)
- Limiting I/O ranges
- Package / image co-design (board / package / image when applicable)

Combinational Cells
- Full family: INV, AND, NAND, OR, NOR, BUF, AO, AOI, OA, OAI, XOR, XNOR, FA, HA, MUX2, MUX4, TIE
- Data-path enhancement family: ADDRs, MAJs, MUXs, others

Clock Cells
- INV, NAND, NOR designed for radiation hardness
- Proper EM consideration for 20 year lifetime
- Glitch-less hardened clock gates for power reduction

Sequential Cells
- D Flip-flops (DFFs) and Latches
- Scan or non-scan, set, reset, set-reset
- With or without Single Event Transient (SET) filters
- Soft latches and DFFs available for non-hardened paths

I/O
- LVCMOS with programmable voltage and drive
- Low power LVCMOS
- SSTL (DDR2 and DDR3 support)
- LVDS
- Schmitt Trigger
- PCI

Support Cells
- Voltage island isolation
- Delay cells
- Antenna cells
- Filler cells
- ESD structures
- E-fuse
Program Objective

- Investigate the use of < 45nm technology to support AMS requirements to include:
  - Very high sample rate (> 25 Gsps) moderate ENOB
  - High sample rate (> 1.5 Gsps) high ENOB
  - Very high sample rate & very low power elemental digital beam forming (eDBF) applications

Technical Approach

- Test and analysis through
  - Critical circuit (e.g., PLL, S/H, etc) design, fabrication, test and characterization
  - Analog to Digital Converter architecture (ADC) Analysis
    - 1-3 bit/ > 20 Gsps W-ADC Arch. Design
    - 10/14 bit/1.5 Gsps W-ADC Evaluation
    - Commercial ADC Benchmark/Qualification
    - High sample rate ADC and digital filter architecture investigation
## Mid/Far Term RHM Program Roadmap

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### Key Milestones:

- **90nm GLOP DSP Prototype**
- **Complete 90nm GLOP T&E**
- **Complete 90nm GFLOP DSP Qualification**
- **Start 45nm GFLOP DSP**
- **Complete 45nm GLOP DSP Prototype**
- **Complete 45nm GFLOP DSP Qualification**
- **Complete 45nm GLOP DSP GLOP T&E**
- **RHBD 45nm ASIC Demonstration & Qualification**
- **RHBD GLOP DSP Demonstration & Qualification**
- **RHBD 45nm Host Bridge & GPP Demonstration & Qualification**
- **RHBD < 45nm AMS Demonstration & Qualification**
- **45nm IP Library Transfer Initiate GPP Design**
- **Complete GPP Design & Fabrication**
- **Complete GPP (5545) Qualification**
- **Complete SBC Qualification**
- **Complete HB Qualification**
- **Complete ESA moon-bit ADC study**
- **Complete Initial ADC study**
- **Complete SIGINT ADC Qualification**
- **Complete COMM Demo**
- **Complete COMM AMS Qualification**
- **Complete ESA ADC Demo**
- **Complete SIGINT AMS Qualification**
Objective:

- Develop and demonstrate Disruptive Technologies for Space Applications
  - High SFDR @ low power CNT FET LNA, Mixer & ADC
  - RH non-volatile & low power memory

Tasks:

- CNT Non-volatile Memory
  - 4Mb/64Mb NRAM
  - 1G DDRX SDRAM

- CNT FET Technology
  - Low power mixer
  - High SFDR ADC
Disruptive Technologies Program Status

Spacecraft Front-end & Processing

CNT FET LNA + Mixer + ADC

- 1000X reduction in power @ > 40dbm SFDR
  When compared to traditional semiconductor technologies

- CNT 4M NRAM Demo 2QFY12
- 64M NRAM FY14
- 1G SDRAM FY16
Improvement in the Frequency Performance of CNT FETs

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- 8 μm Channel
- 3 μm Channel
Why CNT Technology?
- Rad hard
- Non-volatile storage
- High switch speed
- Highly scalable
- Easily integrated into silicon technology
- ~ zero leakage current
- Low interconnect resistance
- Highly linear operation @ low power for mixers & LNA applications

CNT FET Technology to support memory demonstrations (w/ ~ 30% increase in density) and analog mixed-signal circuit development
4Mb NRAM® Description

- Fabricated on 8” wafer
- 67 usable die per wafer for wafer-scale testing and/or packaging 4Mb test chips
- 8-1Mb NRAM® arrays with up to 4-1Mb arrays used for error detection and correction
- 32 databit I/O architecture
- Test register implementation to accommodate standard and multiple special test and debug modes
- Significant enhancements to improve operability and function from 1Mb test chip predecessor

First packaged parts in testing
NRAM functional verification

64 NRAM® bits tested per data point

Multiple die and array tested to verify NRAM® operability

Consistent 100% w0 yield (OFF) performance

w1 yield (ON) performance; > 95% yield across die
Memory Development Tasks

64Mb NRAM Design Complete

DDR2 SDRAM Design In-progress

CNT NRAM

Figure 4: Block diagram of the 64Mb NRAM design, showing 8Mb sub-block arrangement
Summary

- The RHM Program is addressing DoD and IC RH microelectronics needs through a variety of technical thrusts:
  
  - Near term P&Q, Yield enhancement and optimization tasks are underway to exploit 250nm, 180nm and 150nm technologies at BAE Systems and Honeywell
  
  - Mid-term efforts to adopt advanced commercial technologies, e.g., DSP, FPGA, microprocessors, for space system applications, i.e., redesign to address radiation effects, power restrictions and reliability.
  
  - Mid to Far term investigate and demonstrate the use of highly scaled & disruptive technologies, e.g., CNT, to support various spacecraft applications, e.g., OBP, ESA enablement, DSU.
NATIONAL RECONNAISSANCE OFFICE

VIGILANCE FROM ABOVE